


# Politechnika Wrocławska

## Technika cyfrowa 2

### wykład 12

#### Pamięci procesorów


Katedra Metrologii Elektronicznej i Fotonicznej  
Andrzej Stępień



# Pamięć ulotna RAM

**Pamięć ulotna RAM (Volatile Random Access Memory):**

- pamięć o dostępie swobodnym, **utrata** zawartości w momencie zaniku napięcia zasilania Vcc
- **SRAM** (Static RAM):
  - przerzutnik bistabilny jako element pamięciowy
  - brak cykli odświeżania
  - większa (~4 razy) powierzchnia od pamięci DRAM o tej samej pojemności
  - szybsza w stosunku do pamięci dynamicznej
- **DRAM** (Dynamic RAM)
  - kondensator jako element pamięciowy
  - odświeżanie (refresh) ładunku (upływność) kondensatora
  - małe rozmiary



# Pamięć nieulotna NVRAM


**Pamięć nieulotna NVRAM (Non-Volatile Random Access Memory)**

- pamięć o dostępie swobodnym, **zachowanie** zawartości w momencie zaniku napięcia zasilania Vcc
  - pamięci ferrytowe używane w latach 50. i 60. XX wieku
  - pamięci z podtrzymaniem baterijnym
  - NRAM - technologia nanorurek węglowych
  - MRAM – magnetyczny efekt tunelowy magnetycznego
  - OUM - zmiany stanu stopów pierwiastków rudotwórczych (analogia do płyt CD, DVD – zapis/kasowanie za pomocą lasera, zmiana stanu z krystalicznego na amorficzny)
  - FRAM - właściwości ferromagnetyczne



# Pamięć ROM (Read-Only Memory)


- tylko odczyt, brak wpływu napięcia zasilania Vcc na zawartość pamięci
- **ROM** - programowane przez producenta pamięci w czasie produkcji (MROM - Mask programmable ROM)
- **PROM** (Programmable ROM) - pamięć 1-krotnego zapisu (programowania); programowane przez przepalenie połączeń struktury wewnętrznej
- **EPROM** (Electrically Programmable ROM) - pamięć, programowalna elektrycznie, kasowana innymi metodami np. przez naświetlanie światłem ultrafioletowym o wysokiej energii
- **OTP EPROM** (One-Time Programmable EPROM) - pamięć EPROM 1-krotnie programowalna (brak okienka)
- **EEPROM** (Erasable Electrically Programmable ROM) - pamięć wielokrotnego zapisu, kasowalna i programowalna elektrycznie
- **Flash EEPROM** – zapis / kasowanie wielu (bloków) komórek pamięci podczas jednej operacji programowania



# Memory Attributes

*APPLICATION NOTE 63. Using Nonvolatile Static RAMs. Dallas Semiconductor, Mar 29, 2001*

Type	Cost	Ease of Interface	Non-volatile	Density	Performance	Read / Write	Data Retention
Static RAM	+++		+	+++	+++		
DRAM	+++			+++	++	+++	
PSEUDO STATIC RAM	+	+		++	+	+++	
NV SRAM		+++	++	+	+++	+++	++
Flash	++	++	++	++	++	+	++
EEPROM	+	++	+	+		+	+
EPROM	++	++	++	++	+		++
OTP EPROM	+++	+++	+++	+++	+		+++
ROM	+++	+++	+++	+++	+		+++



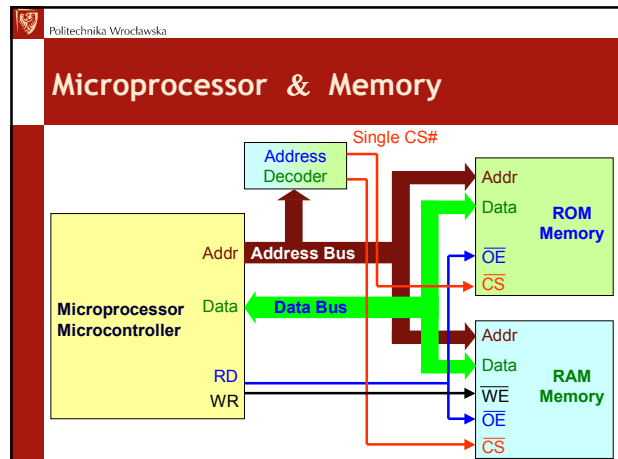
# Memory Parameter (www.st.com → Memories)

- **Memory Size** – [Storage Capacity] The amount of data that can be contained in a storage device measured in binary characters, bytes, words, or other units of data. IEEE Std. 610.10-1994.
- **Supply Voltage** ( $V_{CC}$ ) - the value as specified by level (minTypMax) of the direct supply voltage, applied to an IC. IEC61360-AAE690 ( $V_{CC}$ ).
- **Memory Organization** - Shown as a text representation of the Memory Organization (i.e. 512 x 8).
- **Access Time** ( $t_{ACC}$ ) - time of address to output delay.
- **Chip Enable** To Output Delay ( $t_{CE}$ ) - time of chip enable to output delay.
- **Output Enable** To Output Delay ( $t_{OE}$ ) - time of output enable to output delay.
- **Programming Voltage** ( $V_{PP}$ ) / **Current** ( $I_{PP}$ ) - Programming voltage or current by the specified test condition
- **Standby Supply Voltage Current** CMOS ( $I_{CC2}$ ) - Operating supply current by the specified test condition.
- **Operating Temperature** - The value as specified by level (minTypMax) of the ambient temperature (in Cel) in which this item was designed to operate

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## Memory - Signal Names

- $V_{CC}$  – Supply Voltage
- $V_{SS}$  – Ground
- $V_{PP}$  – Program Supply
- $A_0 \dots A_{XX}$  (Addr) – Address Inputs
- $D_0 \dots D_{XX}$  or  $Q_0 \dots Q_{XX}$  (Data) – Data Inputs / Outputs
- $\overline{RD}$  – Data Read
- $\overline{WR}$  – Data Write
- $\overline{CS}$  or  $\overline{E}$  – Chip Enable
- $\overline{OE}$  or  $\overline{G}$  – Output Enable
- $\overline{P}$  – Program
- $NC$  – Not Connected Internally
- $DU$  – Don't Use



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## Single CS SRAM & dual CS SRAM

**TN419803. BENEFIT OF DUAL CS. TECHNICAL NOTE**  
SAMSUNG Electronics CO., LTD. 1998

- If system has more than one SRAM or controller can not drive CS to high at power down mode, you need additional component on PCB for Data Retention mode
- if you take dual CS products, you can reduce board area because you do not need additional component
- Dual CS products represent flexibility of system design, which adopt battery backup mode

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## Single CS SRAM

**TN419803. BENEFIT OF DUAL CS. TECHNICAL NOTE**  
SAMSUNG Electronics CO., LTD. 1998

Figure 2 Block diagram

Table 2

Single CS	Dual CS		OE	WE	I/O	Mode	Power
CS	CS <sub>1</sub>	CS <sub>2</sub>					
H	H	X <sup>(1)</sup>	X <sup>(1)</sup>	X <sup>(1)</sup>	High-Z	Deselected	Standby
	X <sup>(1)</sup>	L					
L	L	H	H	H	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	Read	Active
L	L	H	X <sup>(1)</sup>	L	Din	Write	Active

1 X means don't care (Must be in low or high state)

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## SRAM (Static Random Access Memory)

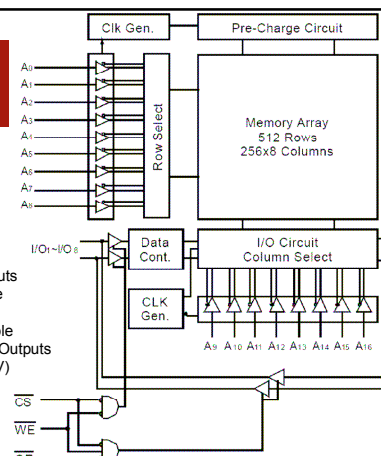
- SRAM is essentially a stable DC flip-flop requiring no clock timing or refreshing.
- The contents of an SRAM memory are retained as long as power is supplied.
- SRAMs support extremely fast access times.
- SRAMs also have relatively few strict timing requirements and a parallel address structure, making them particularly suited for cache and other low-density, frequent-access applications.

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## NV SRAM (NonVolatile Static Random Access Memory)

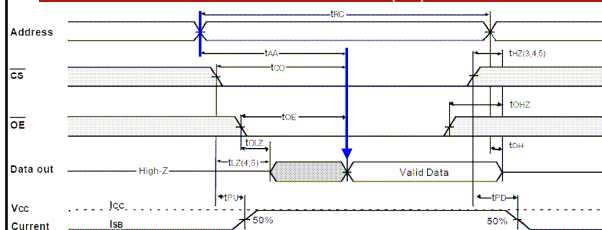
- An NV SRAM is a single package which contains a low-power SRAM, a nonvolatile memory controller, and a lithium type battery.
- When the power supply to this single modular package falls below the minimum requirement to maintain the contents of the SRAM, the memory controller in the module switches the power supply from the external source to the internal lithium battery and write protects the SRAM.
- These transitions to and from the external power source are transparent to the SRAM, making it a true nonvolatile memory.
- This unique construction combines the strategic advantages of SRAM—addressing structure, high-speed access, and timing requirements—with the nonvolatility advantages of EEPROM technologies.
- Battery-backed SRAM modules from Dallas Semiconductor are pin-compatible with non-battery-backed SRAMs, making them ideal for any application where a traditional SRAM would be suitable.

A0 - A16	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
VCC	Power(+3.3V)
VSS	Ground

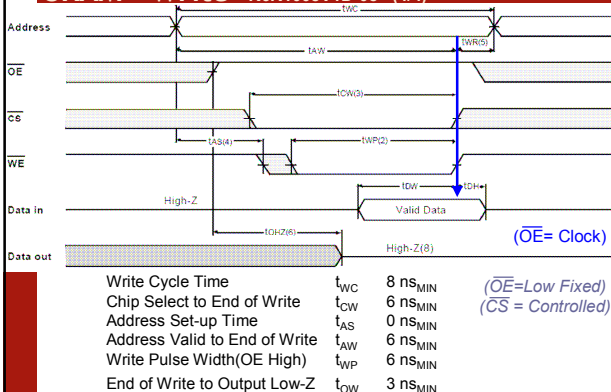


Parameter	Symbol	Test Conditions	Max
Operating Current	$I_{CC}$	Commercial	80 mA
		8ns	65 mA
		10ns	90 mA
		Industrial	75 mA
Standby Current	$I_{SB}$	Min. Cycle, $CS = V_{IH}$	20 mA (TTL)
		$I_{SB1}$ f=0MHz,	5 mA (CMOS)
		$CS \geq V_{CC} - 0.2V$ ,	
		$V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	

Input/Output Capacitance			
	$C_{I/O}$	$V_{I/O}=0V$	8 pF
Input Capacitance	$C_{IN}$	$V_{IN}=0V$	6 pF



Read Cycle Time	$t_{RC}$	8 ns <sub>MIN</sub>
Address Access Time	$t_{AA}$	8 ns <sub>MAX</sub>
Chip Select to Output	$t_{CO}$	8 ns <sub>MAX</sub>
Output Enable to Valid Output	$t_{OE}$	4 ns <sub>MAX</sub>
Output Hold from Address Change	$t_{OH}$	3 ns <sub>MIN</sub>
Chip Selection to Power Up Time	$t_{PU}$	0 ns <sub>MIN</sub>
Chip Selection to Power Down Time	$t_{PD}$	8 ns <sub>MAX</sub>



**K6F1008V2C. 128Kx8 bit Super Low Power and Low Voltage CMOS Static RAM. Samsung Electronics, March 2005**

Parameter	Symbol	K6R1008V1D-08	K6F1008V2C-55
Operating Current	$I_{CC2}$ $I_{CC1}$	90 mA	35 mA <sub>MAX</sub> TTL 3 mA <sub>MAX</sub> CMOS
Standby Current	$I_{SB}$ $I_{SR1}$	20 mA 5 mA	5 $\mu$ A <sub>MAX</sub> TTL 5 $\mu$ A <sub>MAX</sub> CMOS

Input/Output Capacitance		
$C_{I/O}$	8 pF <sub>MAX</sub>	10 pF <sub>MAX</sub>
Input Capacitance		
$C_{IN}$	6 pF <sub>MAX</sub>	8 pF <sub>MAX</sub>

## Memory & Memory (2/2)

**K6R1008V1D. 1Mb Asynchronous Fast SRAM High-Speed CMOS Static RAM. Samsung Electronics June 2003**

**K6F1008V2C. 128Kx8 bit Super Low Power and Low Voltage CMOS Static RAM. Samsung Electronics, March 2005**

		K6R1008V1D-08	K6F1008V2C-55
Read Cycle Time	$t_{RC}$	8 ns <sub>MIN</sub>	55 ns <sub>MIN</sub>
Address Access Time	$t_{AA}$	8 ns <sub>MAX</sub>	55 ns <sub>MAX</sub>
Chip Select to Output	$t_{CO}$	8 ns <sub>MAX</sub>	55 ns <sub>MAX</sub>
Output Enable to Valid Output	$t_{OE}$	4 ns <sub>MAX</sub>	25 ns <sub>MAX</sub>
Output Hold from Address Change	$t_{OH}$	3 ns <sub>MIN</sub>	10 ns <sub>MIN</sub>
Write Cycle Time	$t_{WC}$	8 ns <sub>MIN</sub>	55 ns <sub>MIN</sub>
Chip Select to End of Write	$t_{CW}$	6 ns <sub>MIN</sub>	45 ns <sub>MIN</sub>
Address Set-up Time	$t_{AS}$	0 ns <sub>MIN</sub>	0 ns <sub>MIN</sub>
Address Valid to End of Write	$t_{AW}$	6 ns <sub>MIN</sub>	45 ns <sub>MIN</sub>
Write Pulse Width(OE High)	$t_{WP}$	6 ns <sub>MIN</sub>	40 ns <sub>MIN</sub>
End of Write to Output Low-Z	$t_{WZ}$	3 ns <sub>MIN</sub>	5 ns <sub>MIN</sub>

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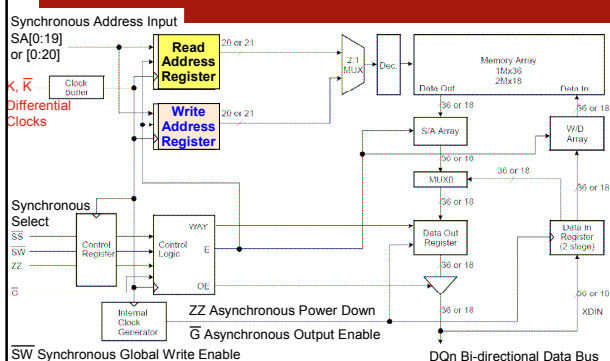
**K7P323688M / K7P321888M.**

**1Mx36 & 2Mx18 Synchronous Pipelined SRAM**  
SAMSUNG Electronics CO., LTD.

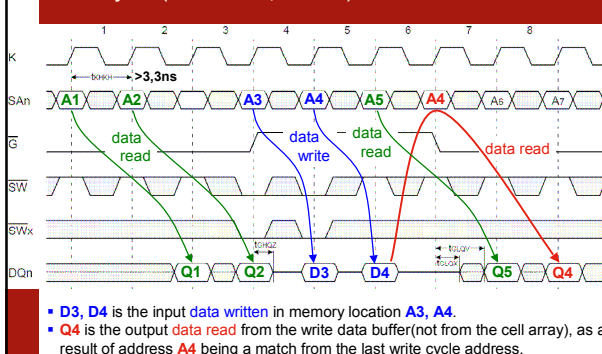
- **Pipeline** - a method of increasing the performance by using multistage circuitry to temporally register the data and convey them while new data is being accessed. The terminology is given based on the fact that the device conveys a train of inputs and outputs like a pipeline.
- **Flow-through** - a SRAM operation mode in which addresses and control signals must be set up before a cycle begins and the data appears at the outputs within the same cycle.

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### Synchronous Pipelined SRAM Functional Block Diagram

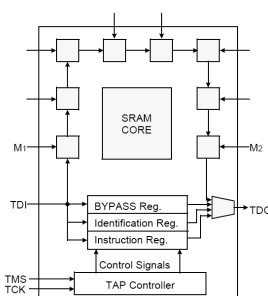
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### Synchronous Pipelined SRAM Timing Waveforms of Normal Active Cycles ( $\overline{G}$ Controlled, $\overline{SS}$ =Low)

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Synchronous Pipelined **SRAM** IEEE 1149.1 Test Access Port & Boundary SCAN-JTAG

### JTAG Block Diagram



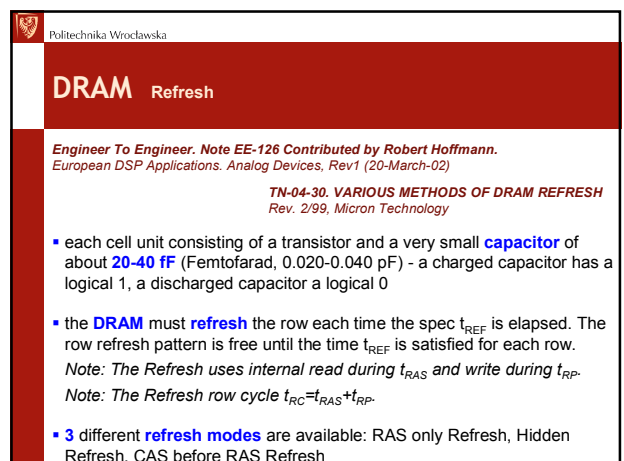
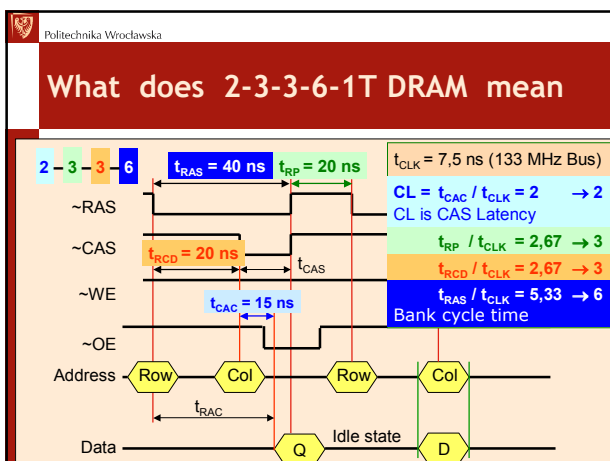
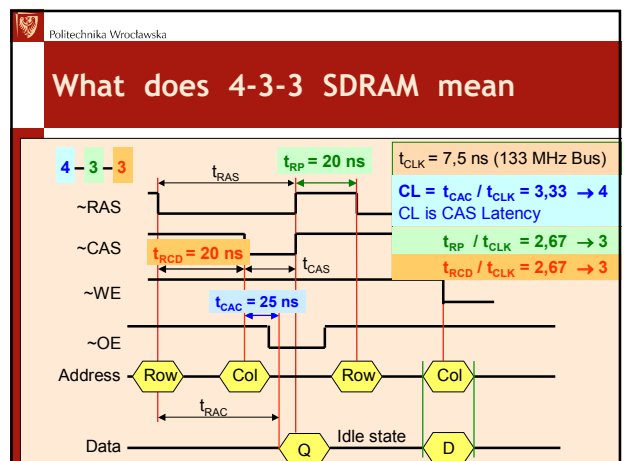
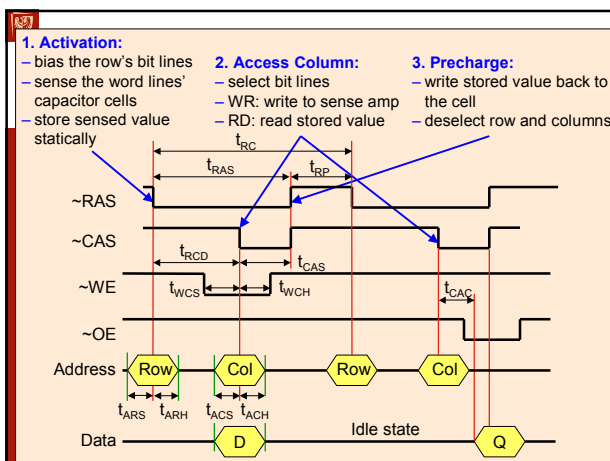
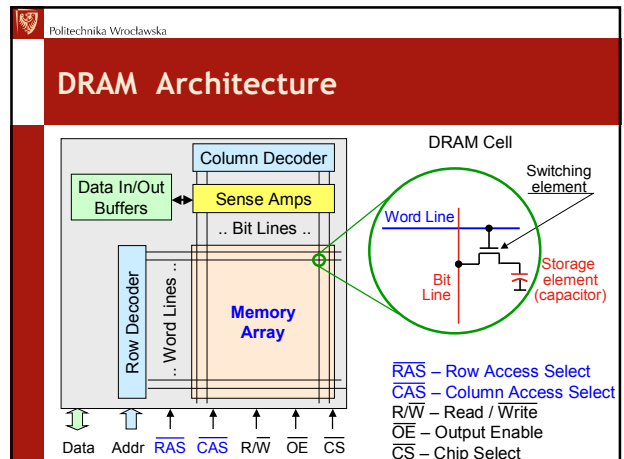
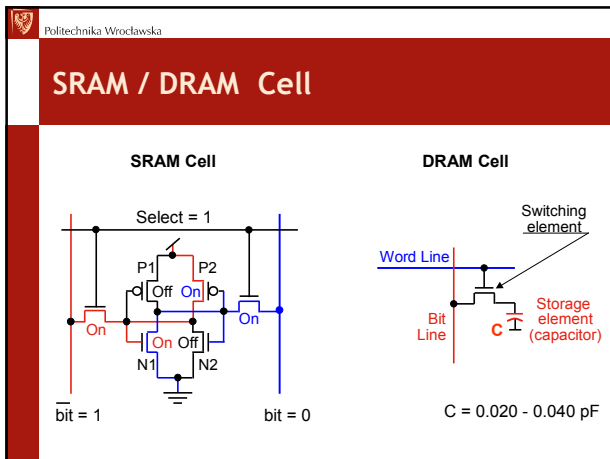
SCAN-JTAG to test the connectivity during manufacturing between SRAM, printed circuit board and other components

TCK	JTAG Test Clock
TMS	JTAG Test Mode Select
TDI	JTAG Test Data Input
TDO	JTAG Test Data Output
M1, M2	Read Protocol Mode Pins

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## DRAM (D<sub>ynamic</sub> R<sub>andom</sub> A<sub>ccess</sub> M<sub>emory</sub>)

- In an SRAM, this information is stored in a four to six transistor flip-flop which is easy to address, but requires a relatively large memory cell.
- DRAM, by comparison, stores its 1 or 0 as a charge on a small capacitor, requiring much more current than an SRAM to maintain the stored data.
- The net memory cell size is smaller for the DRAM than for the SRAM, so the total cost per bit of memory is less.
- The DRAM's capacitors must be constantly refreshed so that they retain their charge.
- DRAMs require more sophisticated interface circuitry.



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## DRAM RAS only Refresh (ROR)

The **external row address** during the falling edge of the  $\sim$ RAS pin starts a refresh each time it is required.  
**Note:** The RAS only refresh requires an external address counter.

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## DRAM CAS before RAS Refresh (CBR)

The **CBR- or auto refresh** is started by deassertion of  $\sim$ CAS followed by the deassertion of  $\sim$ RAS, that means in reversed order. Hereby, the device requires **no external address** to full fill a refresh. The **internal refresh counter** will handle this job.  
**Note:** The CBR refresh is comfortable and reduces the power dissipation.

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## DRAM hidden Refresh

**Hidden Refresh** - The external row address (falling edge of  $\sim$ RAS) and column address (falling edge of the  $\sim$ CAS) starts an internal hidden refresh using the **internal refresh counter**, each time it is required.  
**Note:** The Hidden Refresh can only be used for continuous access of DRAM.

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## PSEUDO STATIC RAM

- The advantages of using a Static RAM are the simplicity of the interface circuitry required, and the fact that the device is by nature "static," not requiring periodic refreshing to retain its data.
- A DRAM, however, provides lower cost-per-bit advantages and a higher memory density.
- A Pseudo-static RAM combines the advantages of the SRAM and DRAM by using dynamic storage cells to retain memory, and by placing all the required refresh logic on-chip so that the device functions similarly to an SRAM.

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## EPROM / OTP EPROM

- EPROM** (Electrically Programmable Read Only Memory) is a nonvolatile memory which offers the ability to both program and erase the contents of the memory multiple times.
- An EPROM must be **programmed** using a **12.5 volt** (or higher) PROM programmer, and then transferred into the system in which it is intended to function.
- EPROMs can be **erased** by shining **ultraviolet light** into the window in the top of the IC package. The process of writing data into an EPROM and then erasing it may be repeated almost indefinitely. EPROMs are usually used for product development, and later replaced with less expensive one-time programmable EPROMs.
- OTP EPROM:** One-Time Programmable EPROM. An EPROM which can only be written with code/data once instead of multiple times. Generally, OTP EPROMs are less expensive than erasable EPROMs.

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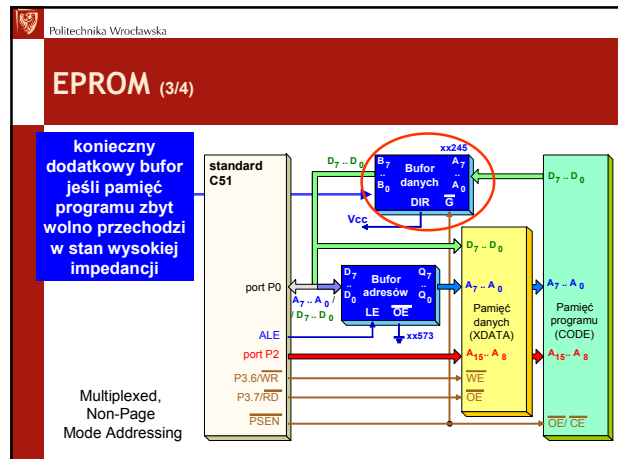
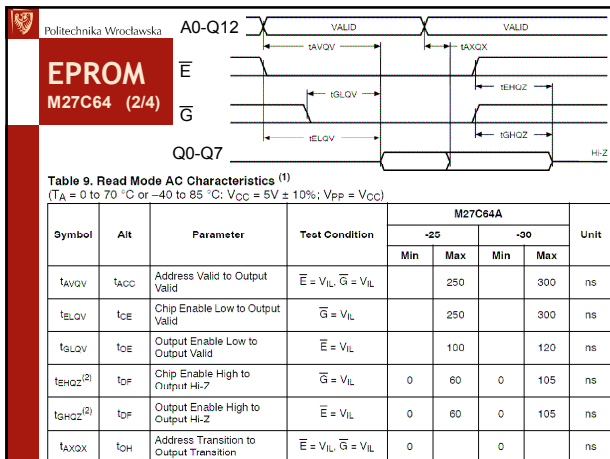
## EPROM M27C64 (1/4)

**M27C64A. 64 Kbit (8Kb x8) UV EPROM and OTP EPROM. STMicroelectronics, October 2002**

Mode	$\bar{E}$	$\bar{G}$	$\bar{P}$	$V_{PP}$	Q Output
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	Data Out
Output Disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{CC}$	Hi-Z
Program	$V_{IL}$	X	$V_{IL}$ Pulse	$V_{PP}$	Data Input
Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{PP}$	Data Output
Standby	$V_{IH}$	X	X	$V_{CC}$	Hi-Z

$C_{IN}$ Input Capacitance	$V_{IN} = 0V$	6 pF <sub>MAX</sub>
$C_{OUT}$ Output Capacitance	$V_{OUT} = 0V$	12 pF <sub>MAX</sub>

$I_{CC}$ Supply Current	$\bar{E} = V_{IL} \quad \bar{G} = V_{IL}$	30 mA <sub>MAX</sub>
$I_{CC1}$ Supply Current (Standby) TTL	$\bar{E} = V_{IH} \quad \bar{G} = X$	1 mA <sub>MAX</sub>
$I_{CC2}$ Supply Current (Standby) CMOS	$E > V_{CC} - 0.2V$	100 $\mu$ A <sub>MAX</sub>



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## EPROM - M27C64 ERASURE OPERATION (4/4a)

- When delivered (and after each erasure for UV EPROM), all bits of the M27C64A are in the "1" state.
- Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.
- The only way to change a "0" to a "1" is by die exposition to ultraviolet light (UV EPROM). The M27C64A is in the programming mode when  $V_{PP}$  input is at 12.5V,  $\bar{E}$  is at  $V_{IL}$  and  $\bar{P}$  is pulsed to  $V_{IL}$ .
- The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.  $V_{CC}$  is specified to be  $6\text{V} \pm 0.25\text{V}$ .

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## EPROM - M27C64 ERASURE OPERATION (4/4b)

### ERASURE OPERATION

- The erasure begins when the cells are exposed to **light with wavelengths shorter than approximately 4000 Å**. It should be noted that sunlight and some type of **fluorescent lamps** have wavelengths in the **3000-4000 Å** range.
- Research shows that constant exposure to **room level fluorescent lighting** could **erase** a typical M27C64A in about **3 years**, while it would take approximately **1 week** to cause erasure when exposed to direct **sunlight**.
- The **recommended** erasure procedure for the M27C64A is exposure to short wave ultraviolet light which has a **wavelength of 2537 Å**.
- The integrated dose (i.e. UV **intensity** x exposure time) for erasure should be a minimum of **15 W-sec/cm²**. The erasure time with this dosage is approximately **15 to 20 minutes** using an ultraviolet lamp with **12000 µW/cm²** power rating. The M27C64A should be placed within **2.5 cm** (1 inch) of the lamp tubes during the erasure.

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## EEPROM - Flash Memory

- EEPROM:**
  - erase the entire device all at once
  - program or write single bytes at a time
- Flash** is a high-speed EEPROM:
  - program and erase BLOCKS of data at a time

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## EEPROM - AT25XXX Serial

*AT25128/AT25256, SPI Serial Automotive EEPROMs 128K (16,384 x 8) / 256K (32,768 x 8) doc3262.pdf - Rev. 3262A-SEEPR-02/02, Atmel Corporation 2002.*

- Serial Peripheral Interface (SPI) Compatible
- Medium-voltage and Standard-voltage Operation
  - 5.0 (VCC = 4.5V to 5.5V)
  - 2.7 (VCC = 2.7V to 5.5V)
- 3 MHz Clock Rate
- 64-byte Page Mode and Byte Write Operation
- Block Write Protection – Protect 1/4, 1/2, or Entire Array
- Write Protect (WP) Pin and Write Disable Instructions for both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms Typical)
- High-reliability
  - Endurance: 100,000 Write Cycles
  - Data Retention: >200 Years



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	<b>NAND</b>	<b>NOR</b>
Cell Array		
Layout		
Cross section		
Cell size	$4F^2$	$10F^2$

Figure 1. NAND Flash vs. NOR Flash

**NOR Flash Array**

**NAND Flash Array**

**NAN**

[www.st.com](http://www.st.com): **Challenge The End of the War NAND vs NOR.**

- In the **NOR architecture**, a cell is read by connecting the Source Line to ground, raising the voltage on the Word Line to the sense level and connecting the Bit Line to the sense amplifier; if the cell is programmed, no current flows to the sense amplifier.
- In the **NAND architecture**, the same procedure is followed but the correct group of cells must also be selected using the Bit Line Select inputs
- Today it is possible to build sense amplifiers that can distinguish between four different levels of charge on the floating gate i.e. 2 bits/cell.

## NOR or NAND (1/2) ?

- NOR flash** memory:
  - used to store relatively small amounts of executable code for embedded computing devices (PDAs, cell phones)
  - suited to use for code storage - reliability, fast read operations, and random access capabilities
  - code can be directly executed in place, ideal for storing firmware, boot code, operating systems, and other data (changes infrequently).
- NAND flash** memory:
  - the preferred format for storing larger quantities of data on devices such (USB Flash drives, digital cameras, MP3 players)
  - consumer media applications (large files of sequential data loaded into memory quickly and replaced), higher density, lower cost, and faster write and erase times.

## NOR or NAND (2/2) ?

- NOR flash** memory:
  - the **Random Access** is **possible** and very fast (@ 70 ns)
  - the **Write Time** is the main disadvantage, as it is **slow** (@ 6 μs/Byte and around 3 ms/512 Bytes).
- NAND flash** memory:
  - allows a very **fast Sequential Access** (@ 50 ns), it is **not adapted** for a **random access** (@ 25 μs)
  - are about 40% smaller, and achieves a **higher density** (Sixteen neighbouring cells are serially connected without any contact area in-between)
  - becomes more advantageous than the NOR Flash for the Write Time in bundle (several Bytes together (@ 200 μs/512 Bytes)). It is around **10 times faster** than the NOR Flash.