


Politechnika Wroclawska

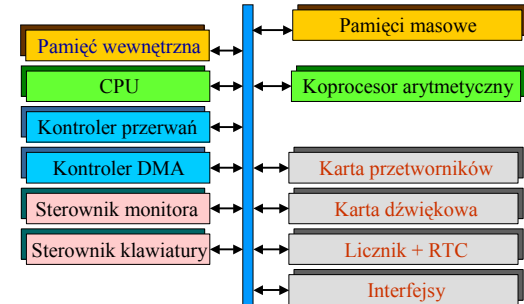
Technika cyfrowa 2


wykład 4

Katedra Metrologii Elektronicznej i Fotonicznej
Andrzej Stępień

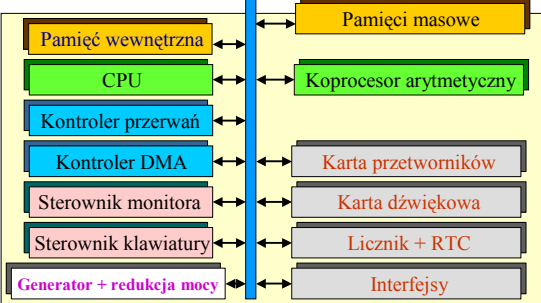



Co zawiera komputer PC ?





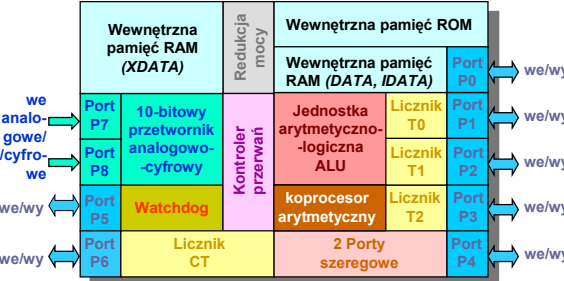
A to jest w mikrokontrolerze






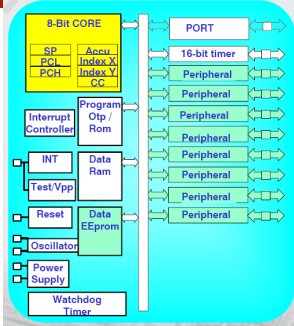
MCS® 51 Family (8 - bit)

'C517A






ST7 Family (8-bit, STMicroelectronics)

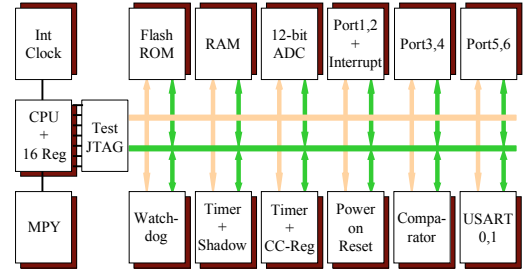


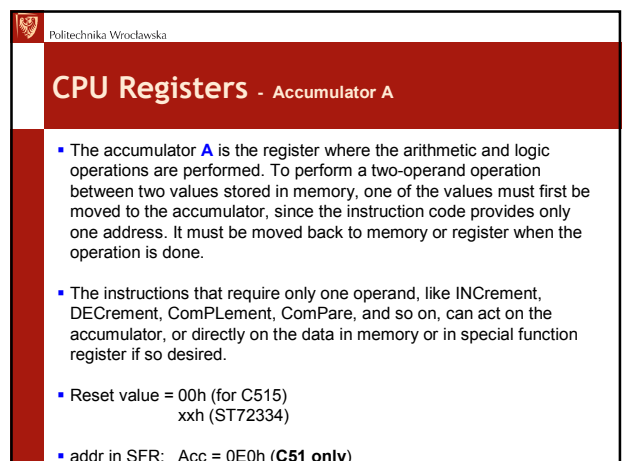
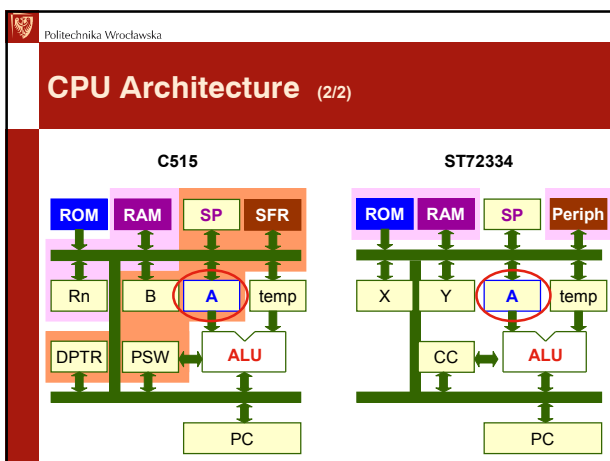
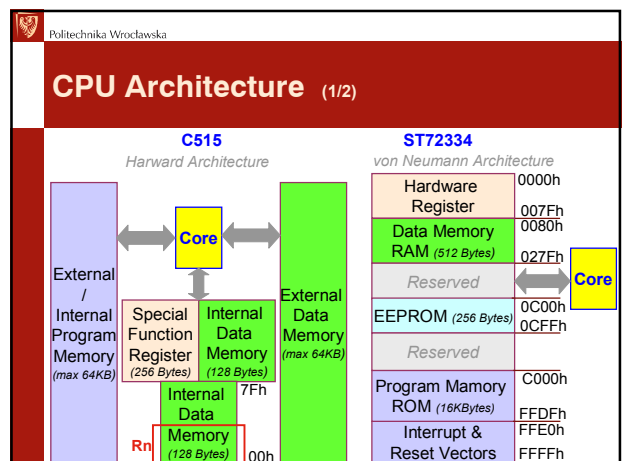
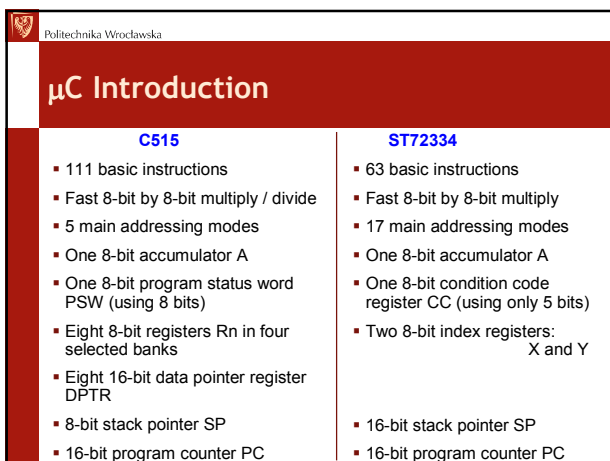
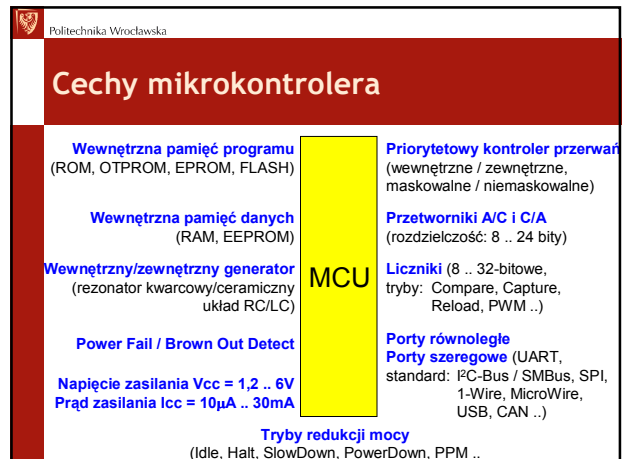
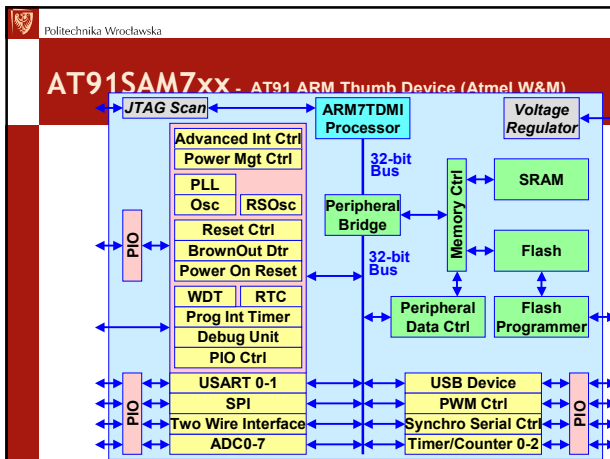
Optional features:

- AD converter
- 16-bit Timer
- 8-bit Auto Reload Timer
- SPI
- SCI
- I2C
- EEPROM
- Programmable OpAmp
- CAN



MSP430F13x/14x Mixed Signal Microcontroller (16 - bit)





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ST72334 CPU Registers - Index Registers (X and Y)

- The index registers **X** and **Y** are meant to hold addresses, unlike the accumulator which is meant to hold data. The value stored in X or Y is involved in the effective address calculation in some addressing modes.
- The availability of two index registers (X and Y) allows for calculating and managing two addresses as is needed in a memory-to-memory data move, with or without alteration in between.
- However, these registers may also be used to store temporary data.
- Reset value = xxh

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C515 CPU Registers - Data Pointer Register

- 8-bit accesses to the internal XRAM data memory or the external data memory or the code memory are executed using the data pointer **DPTR** as an 16-bit address
- addr in SFR: DPL=82h
DPH=83h
- Reset value = 0000h

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ST72334 CPU Registers - Condition Code Register (1/2)

- This register holds several bits that are actually more or less independent from one another.
- These bits are set or reset (or left unchanged) after the execution of certain instructions. For example, if an addition produces a null result, the Z flag is set; otherwise, it is reset. If the result is negative, the N flag is set, otherwise it is reset and so on.
- Reset value = 111X 1XXX

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ST72334 CPU Registers - Condition Code Register (2/2)

The CC register remembers the conditions after each instruction, and these conditions are used by the conditional jump instructions. The CC is laid out as follows:

1	1	1	H	I	N	Z	C
---	---	---	---	---	---	---	---

- H** - Half carry
- I** - Interrupt mask
- N** - Negative
- Z** - Zero
- C** - Carry/borrow

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C515 CPU Registers - Program Status Word Register

- Reset value = 00h
- C** - Carry
- AC** - Auxiliary Carry
- F0** - General purpose user flag 0
- RS1, RS0** - Register Bank select
- OV** - Overflow
- F1** - General purpose user flag 1
- P** - Parity

addr in SFR: 0D0h

CY	AC	F0	RS1	RS0	OV	F1	P
----	----	----	-----	-----	----	----	---

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Condition - cy, c

C515								ST72334							
(CY)	AC	F0	RS1	RS0	OV	F1	P	1	1	1	H	I	N	Z	(C)

- Carry Flag (CY) – C515**
Used by arithmetic (unsigned) and conditional branch instruction.
- Carry/Borrow (C) – ST7**
When set, C indicates that a carry or borrow out of the ALU occurred during the last arithmetic operation on the MSB operation result bit. This bit is also affected during bit test, branch, shift, rotate and load instructions.

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Condition – AC, H

C515

CY	AC	F0	RS1	RS0	OV	EL	P
----	----	----	-----	-----	----	----	---

ST72334

1	1	1	H	1	N	Z	C
---	---	---	---	---	---	---	---

- **Auxiliary Carry Flag (AC) – C515**
Used by instructions which execute BCD operations.
- **Half carry bit (H) – ST7**
The H bit is set to 1 when a carry occurs between the bits 3 and 4 of the ALU during an ADD or ADC instruction. The H bit is useful in BCD arithmetic subroutines.

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Condition – OV, P

C515

CY	AC	F0	RS1	RS0	OV	EL	P
----	----	----	-----	-----	----	----	---

ST72334

1	1	1	H	1	N	Z	C
---	---	---	---	---	---	---	---

- **Overflow Flag (OV) – C515**
Used by arithmetic instruction (signed).
- **Parity Flag (P) – C515**
Always set/cleared by hardware to indicate an odd/even number of "one" bits in the accumulator.

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Condition – I, N, Z

C515

CY	AC	F0	RS1	RS0	OV	EL	P
----	----	----	-----	-----	----	----	---

ST72334

1	1	1	H	1	N	Z	C
---	---	---	---	---	---	---	---

- **Interrupt mask (I)**
When the I bit is set to 1, all interrupts are disabled. Clearing this bit enables them. Interrupts requested while I is set, are latched and can be processed when I is cleared (only one interrupt request per interrupt enable flag can be latched). This bit can be set/reset by software and is automatically set after reset or at the beginning of an interrupt routine.
- **Negative (N)**
When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is negative (i.e. the most significant bit is a logic 1).
- **Zero (Z)**
When set to 1, this bit indicates that the result of the last arithmetic, logical or data manipulation is zero.

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C51 - Addressing Mode (1/2)

- **Immediate Addressing Mode (natychmiastowe):**
`MOV A, #3` ; A ← 3, wartość
- **Register Addressing Mode (rejestrów):**
`MOV A, R1` ; A ← R1, nazwa rejestru
- **Direct Addressing Mode (bezpośrednie):**
`MOV A, 1` ; A ← (1), adres pamięci
- **Indirect Addressing Mode (pośrednie):**
`MOV A, @R1` ; A ← (R1), adres pamięci w R1

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C51 - Addressing Mode (2/2)

- **Indirect Register - Indexed Addressing Mode (rejestrowo-indeksowo-pośrednie):**
`MOVC A, @A+DPTR` ; A ← (A+DPTR), adres pamięci w A+DPTR

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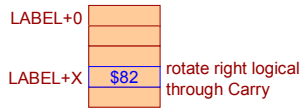
ST7 - Addressing Mode (1/4)

(<http://mcu.st.com/mcu:1117550405.pdf>)

- **Inherent (właściwe):**
`PUSH A` ; (Stack) ← A
- **Short Direct Addressing Mode (bezpośrednie, krótkie):**
`INC LABEL` ; (LABEL) ← (LABEL) + 1
; ADDRESSABLE SPACE: 00 to FF
- **Immediate Addressing Mode (natychmiastowe):**
`LD A, #$55` ; A ← \$55
- **Long Direct Addressing Mode (bezpośrednie długie):**
`ADD A, LABEL` ; A ← A + (LABEL)
; ADDRESSABLE SPACE: 0000 to FFFF


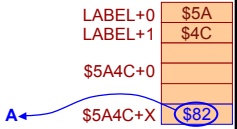
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ST7 - Addressing Mode (2/4)

- **No Offset Indexed Addressing Mode:**
`CPL (X)` ; $(X) \leftarrow \text{NOT}(X)$
- **Short Indexed Addressing Mode:**
`RRC (LABEL, X)` ; $C \rightarrow (LABEL + X) \rightarrow C$

- **Long Indexed Addressing Mode:**
`LD X, (LABEL, X)` ; $X \leftarrow (LABEL + X)$

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ST7 - Addressing Mode (3/4)

- **Short Indirect Addressing Mode:**
`SWAP [LABEL]` ; $\text{SWAP}((LABEL))$

- **Long Indirect Addressing Mode:**
`LD A, [LABEL.w]` ; $A \leftarrow ((LABEL) * 256 + (LABEL + 1))$
- **Short Indirect Indexed Addressing:**
`CLR ([LABEL], X)` ; $((LABEL) + X) \leftarrow 0$
- **Long Indirect Indexed Addressing:**
`LD A, ([LABEL.w], X)` ; $A \leftarrow ((LABEL) * 256 + (LABEL + 1) + X)$


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ST7 - Addressing Mode (4/4)

- **Relative Addressing Mode – Direct / Indirect Addressable Space:**
`JRMI LABEL or JRMI [LABEL]`
 ; Jump Relative: $PC \leftarrow PC + \text{dst}$ if Condition is True (MI = Minus, N=1)
- **Bit Manipulation – Direct / Indirect Addressable Space:**
`BSET variable, #n` ; set bit n in variable
`BRES [variable], #n` ; clear bit n in (variable)
- **Relative Jump On BIT Test – Direct / Indirect Addressable Space:**
`BTJT variable, #n, label` ; jump to LABEL if bit n in variable
`BTJT [variable], #n, label` ; jump to LABEL if bit n in (variable)

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MCS[®]51 na stronach www

- www.8052.com
- www.atmel.com
- www.cygnal.com / www.silabs.com
- www.infineon.com
- www.intel.com
- www.maxim-ic.com
- www.semiconductors.philips.com
- www.st.com ← także **ST7** mcu.st.com/mcu
- www.ti.com

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C51 – typy pamięci

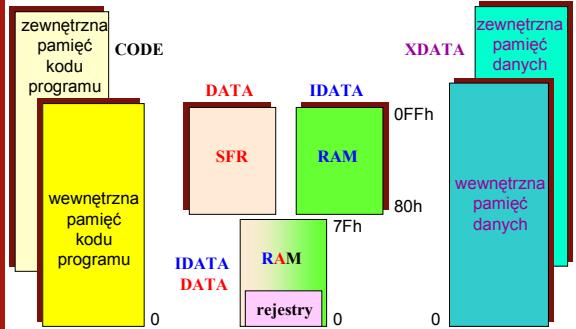


Diagram illustrating memory types and their locations:

- CODE:** zewnętrzna pamięć kodu programu (external), wewnętrzna pamięć kodu programu (internal).
- DATA:** zewnętrzna pamięć danych (external), wewnętrzna pamięć danych (internal).
- IDATA:** wewnętrzna pamięć danych (internal).
- SFR:** Special Function Registers.
- RAM:** wewnętrzna pamięć danych (internal).
- rejestry:** registers.

Address ranges: 0, 7Fh, 80h, 0FFh.

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C51 – adresowanie pamięci danych i kodu

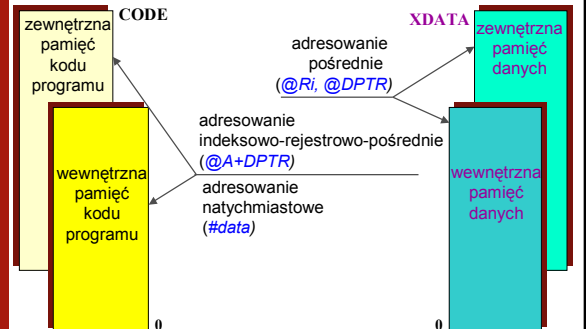


Diagram illustrating memory addressing methods:

- CODE:** zewnętrzna pamięć kodu programu (external), wewnętrzna pamięć kodu programu (internal).
- DATA:** zewnętrzna pamięć danych (external), wewnętrzna pamięć danych (internal).
- IDATA:** wewnętrzna pamięć danych (internal).
- rejestry:** registers.

Addressing methods:

- adresowanie pośrednie ($@R_i$, $@DPTR$)
- adresowanie indeksowo-rejestrowo-pośrednie ($@A+DPTR$)
- adresowanie natychmiastowe ($\#data$)

